Amendments to the Claims

Please cancel Claims 18-32, 50-64, and 66 without prejudice. Applicant reserves the right to re-file these claims in a continuation application. Please amend claims 2, 4, 6-7, 10-11, 35-36, 38-39 and 42 and substitute new claims 67-86 for the cancelled claims. The Claim Listing below will replace all prior versions of the claims in the application:

**Claim Listing**

What is claimed is:

1. (previously presented) A data transmitter comprising:

a data input;

plural delay elements that apply different delays to the data input to provide plural delayed data signals; and

a data output that combines the delayed data signals, a rise or fall transition time of the data output being determined by different delays applied to the data input, wherein the rise or fall transition time of the data output signal is greater than the rise or fall transition time of the data input.

2. (currently amended) A data transmitter as claimed in claim 1 wherein ~~plural of~~ the delay elements are parallel delay elements connected in series with a common delay element.

3. (original) A data transmitter as claimed in claim 1 wherein a clock signal is applied to the delay elements and different delays are applied to the data input by clocking the data input with different delayed clock signals.

4. (currently amended) A data transmitter as claimed in claim 3 wherein the delayed clock signals sequence output from the data input into plural driver circuits.

5. (original) A data transmitter as claimed in claim 4 wherein each delay element comprises CMOS inverters.

6. (currently amended) A data transmitter as claimed in claim 5 wherein delay of [[the]] a respective delay element[[s]] is dependent on its output ~~determined by~~ load capacitance.

7. (currently amended) A data transmitter as claimed in claim 1 wherein the data input is applied in parallel to the delay elements.

8. (original) A data transmitter as claimed in claim 7 wherein an output the delayed data signals are applied to plural driver circuits.

9. (original) A data transmitter as claimed in claim 8 wherein each delay element comprises CMOS inverters.

10. (currently amended) A data transmitter as claimed in claim 9 wherein delay of [[the]] a respective delay element[[s]] is ~~determined by~~ load capacitance.

11. (currently amended) A data transmitter as claimed in claim 1 wherein the transition time of the data output is proportional to bit time associated with a bit clock.

12. (original) A data transmitter as claimed in claim 1 wherein supply voltage to the delay elements is controlled to control delay of the delay elements.

13. (original) A data transmitter as claimed in claim 12 further comprising a circuit to control the supply voltage to the delay elements, the circuit comprising:

first and second delay elements, each receiving a common clock signal; and

a phase comparator which compares outputs of the first and second delay elements and controls a supply voltage applied to the first and second delay elements to control phase difference of the outputs.

14. (original) A data transmitter as claimed in claim 13 wherein each of the first and second delay elements comprises a sequence of n elements and the clock signal frequency is 1/n times bit rate.

15. (original) A data transmitter as claimed in claim 12 wherein the supply voltage is varied to compensate for environmental changes in delay.

16. (Previously presented) A data transmitter as claimed in claim 1 further comprising a circuit to control supply voltage to the delay elements, the circuit comprising:

first and second delay elements, each receiving a common clock signal; and

a phase comparator which compares outputs of the first and second delay elements and controls the supply voltage applied to the first and second delay elements to control phase difference of the outputs.

17. (original) A data transmitter as claimed in claim 16 wherein each of the first and second delay elements comprises a sequence of n elements and the clock signal frequency is 1/n times bit rate.

18-32 (cancelled)

33. (previously presented) A method of transmitting data comprising:

applying different delays to a data input to provide plural delayed data signals; and

combining the plural delayed data signals to provide a data output having a rise or fall transition time determined by different delays applied to the data input, wherein the

rise or fall transition time of the data output signal is greater than the rise or fall transition time of the data input.

34. (original) A method as claimed in claim 33 wherein the different delays are obtained by applying a first delay to the data input and further delaying in parallel delay elements.

35. (currently amended) A method as claimed in claim [[34]] 33 wherein a clock signal is applied to the delay element[[s]] to generate different delayed clock signals and different delays are applied to the data input by clocking the data input with the different delayed clock signals.

36. (currently amended) A method as claimed in claim 35 wherein the delayed clock signals sequence output from the data input into plural driver circuits.

37. (original) A method as claimed in claim 36 wherein each delay is obtained in CMOS inverters.

38. (currently amended) A method as claimed in claim 37 wherein delay of [[the]] a delay respective element[[s]] dependant on its output is ~~determined by~~ load capacitance.

39. (currently amended) A method as claimed in claim 34 wherein an output from the data input is applied in parallel to the delay elements.

40. (original) A method as claimed in claim 39 wherein the delay data signals are applied to plural driver circuits.

41. (original) A method as claimed in claim 40 wherein each delay element comprises CMOS inverters.

42. (currently amended) A method as claimed in claim 41 wherein delay of [[the]] a delay respective element[[s]] dependant on its output is ~~determined by~~ load capacitance.

43. (original) A method as claimed in claim 33 wherein the transition time of the data output is proportional to bit time.

44. (previously presented) A method as claimed in claim 34 further comprising controlling supply voltage to the delay elements to control delay of the delay elements.

45. (original) A method as claimed in claim 44 wherein the supply voltage to the delay elements is controlled by:

applying a common clock signal to first and second delay elements; and

comparing outputs of the first and second delay elements and controlling the supply voltage applied to the first and second delay elements to control phase difference of the output.

46. (original) A method as claimed in claim 45 wherein each of the first and second delay elements comprises a sequence of n elements and the clock signal is 1/n bit rate.

47. (original) A method as claimed in claim 44 wherein the supply voltage is varied to compensate for environmental changes in delay.

48. (Previously presented) A method as claimed in claim 34 wherein supply voltage to the delay elements is controlled by:

applying a common clock signal to first and second delay elements; and

comparing outputs of the first and second delay elements and controlling the supply voltage applied to the first and second delay elements to control phase difference of the outputs.

49. (original) A method as claimed in claim 48 wherein each of the first and second delay elements comprises a sequence of n elements and the clock signal frequency is 1/n times bit rate.

50-64 (cancelled)

65. (previously presented) A data transmitter comprising:

a data input;

plural delay means for applying different delays to the data input to provide plural delayed data signals; and

data output means for combining the delayed data signals into a data output having a rise or fall transition time determined by different delays applied to the data input, wherein the rise or fall transition time of the data output signal is greater than the rise or fall transition time of the data input.

66. (cancelled)

67. (new) A data transmitter as claimed in claim 1, wherein the data input includes plural sampling elements , and wherein the plural delay elements apply different delays to the data input by applying different delays to an input clock to generate sequencing clock signals that are applied to respective ones of the plural sampling elements.

68. (new) A data transmitter as claimed in claim 67 wherein each sampling element samples input data according to a respective one of the sequencing clocks.

69. (new) A data transmitter as claimed in claim 68 wherein each sampling element includes one of the group consisting of latches, flip-flops, and multiplexers.

70. (new) A data transmitter as claimed in claim 67 wherein the sequencing clocks have a spacing that is much less than delay of one of the delay elements.

71. (new) A data transmitter as claimed in claim 70 wherein the spacing is dependent on a difference between delays of two of the delay elements.

72. (new) A data transmitter as claimed in claim 1 wherein the data input includes a sampling element, and wherein the plural delay elements apply different delays to the data input by applying different delays to an output of the sampling element.

73. (new) A data transmitter as claimed in claim 72, wherein the sampling element includes one of the group consisting of latches, flip-flops, and multiplexers.

74. (new) A data transmitter as claimed in claim 1 wherein the plural delay elements include a parallel arrangement of delay elements that apply different delays to a data signal sampled by the data input to provide the plural delayed data signals.

75. (new) A data transmitter as claimed in claim 6, wherein the output load capacitance of a respective delay element is chosen so that an increment in delay corresponds to a required fraction of a bit time associated with a bit clock.

76. (new) A data transmitter as claimed in claim 10, wherein the output load capacitance of a respective delay element is chosen so that an increment in delay corresponds to a required fraction of a bit time associated with a bit clock.

77. (new) A method as claimed in claim 33, wherein the data input includes plural sampling elements and the step of applying includes applying different delays to an input clock to generate sequencing clock signals that are applied to respective ones of the plural sampling elements.

78. (new) A method as claimed in claim 77 wherein each sampling element samples input data according to a respective one of the sequencing clocks.

79. (new) A method as claimed in claim 78 wherein each sampling element includes one of the group consisting of latches, flip-flops, and multiplexers.

80. (new) A method as claimed in claim 77 wherein the sequencing clocks have a spacing that is much less than delay of one of the delay elements.

81. (new) A method as claimed in claim 80 wherein the spacing is dependent on a difference between delays of two of the delay elements.

82. (new) A method as claimed in claim 33 wherein the data input includes a sampling element, and wherein the step of applying includes applying different delays to an output of the sampling element.

83. (new) A method as claimed in claim 82, wherein the sampling element includes one of the group consisting of latches, flip-flops, and multiplexers.

84. (new) A method as claimed in claim 33 wherein the step of applying includes applying different delays to a data signal sampled by the data input to provide the plural delayed data signals.

85. (new) A method as claimed in claim 38 wherein the output load capacitance of a respective delay element is chosen so that an increment in delay corresponds to a required fraction of a bit time associated with a bit clock.

86. (new) A method as claimed in claim 42 wherein the output load capacitance of a respective delay element is chosen so that an increment in delay corresponds to a required fraction of a bit time associated with a bit clock.